Claims

What is claimed is:

1. A clock repeater for regenerating a clock signal on a clock distribution line, comprising:

an edge detector means for sensing a rising edge and a falling edge of said clock signal and generating respective pull-up and pull-down control signals in response thereto; and

an output driver means, connected to said edge detector means to receive said control signals therefrom, for recovering high and low logical levels of said clock signal.

2. The clock repeater of claim 1, wherein said edge detector means further comprises:

a level detector means for generating a first signal and a second signal by detecting a rise edge from a low logical level and a fall edge from a high logical level of said clock signal;

a first logic NOR gate adapted to receive an inverse of the first signal and an inverse of the second signal;

a second logic NOR gate adapted to receive the first signal and the second signal;

a set/reset latch coupled to an output of the first logic NOR gate at a set input terminal, and an output of the second logic NOR gate at the reset input terminal to produce a third signal;

a first logic NAND gate adapted to receive the first signal, the inverse of the second signal to generate the pull-up control signal; and

a third logic NOR gate adapted to receive the inverse of the first signal, the second signal, and the third pulse signal to generate the pull-down control signal.

3. The clock repeater of claim 2, wherein said level detector means further comprises a first level detector means for detecting said high logical level and a second level detector means for detecting said low logical level of said clock signal.

4. The clock repeater of claim 3, wherein said first level detector means further comprising:

a low-threshold PMOS transistor and a high-threshold NMOS transistor for detecting said high logical level of said clock signal, wherein the gate of said low-threshold PMOS transistor and the gate of said high-threshold NMOS transistor being coupled together and to said clock signal, the drain of said low-threshold PMOS transistor being coupled to the drain of the high-threshold NMOS transistor, the source of said low-threshold PMOS being coupled to a supply voltage, and the source of said high-threshold NMOS transistor being coupled to an electrical ground; and

a first inverter having an input terminal coupled to the drain-drain junction of said low-threshold PMOS transistor and said high-threshold NMOS transistor to produce the said first signal, wherein the output terminal of said first inverter being the inverse of said first signal.

5. The clock repeater of claim 3, wherein said second level detector means further comprises:

a high-threshold PMOS transistor and a low-threshold NMOS transistor for detecting said low logical levels of said clock signal, wherein the gate of said high-threshold PMOS transistor and the gate of said low-threshold NMOS transistor being coupled together, the drain of said high-threshold PMOS transistor being coupled to the drain of the low-threshold NMOS transistor, the source of said high-threshold PMOS transistor being coupled to said supply voltage, and the source of said low-threshold NMOS transistor being coupled to said electrical ground; and

a second inverter having an input terminal coupled to the drain-drain junction of the high-threshold PMOS transistor and said low-threshold NMOS transistor to produce said second signal, wherein the output terminal of said second inverter being the inverse of said second signal.

6. The regenerative clock repeater of claim 1, wherein said output driver means further comprises:

a pull-up PMOS transistor;

a NMOS pull-down transistor coupled to said pull-up PMOS transistor, wherein the gate of the said PMOS pull-up transistor being coupled to said pull-up control signal, the drain of said pull-up PMOS transistor being coupled to the drain of the NMOS pull-down transistor and to said clock signal, the source of the PMOS pull-up transistor being coupled to said voltage supply, a gate of the NMOS pull-down transistor being coupled to said pull-down control signal, and the source of said pull-down NMOS transistor coupled to said electrical ground.

7. A clock repeater for regenerating a clock signal on a clock distribution line, comprising:

(a) an edge detector means for sensing a rising edge and a falling edge of said clock signal and generating respective pull-up and pull-down control signals in response thereto; and

(i) a level detector means for generating a first signal and a second signal by detecting a low logical level and a high logical level of said clock signal;

(ii) a first logic NOR gate adapted to receive an inverse of the first signal and an inverse of the second signal;

(iii) a second logic NOR gate adapted to receive the first signal and a second signal;

(iv) a set/reset latch coupled to the output of the first logic NOR gate at a set input terminal, and the output of the second logic NOR gate at the reset input terminal to produce a third signal;

(v) a first logic NAND gate adapted to receive the first signal, the inverse of the second signal to generate the pull-up control signal; and

(vi) a third logic NOR gate adapted to receive the inverse of the first signal, the second signal, and the third pulse signal to generate the pull-down signal;

(b) an output driver means, connected to said edge detector means to receive said control signals therefrom, for recovering high and low logical levels of said clock signal;

(i) a pull-up PMOS transistor;

(ii) a NMOS pull-down transistor coupled to said pull-up PMOS transistor, wherein the gate of the said PMOS pull-up transistor being coupled to said pull-up control signal, the drain of said pull-up PMOS

transistor being coupled to the drain of the NMOS pull-down transistor and to said input clock signal, the source of the PMOS pull-up transistor being coupled to said voltage supply, a gate of the NMOS pull-down transistor being coupled to said pull-down control signal, and the source of said pull-down NMOS transistor coupled to said electrical ground.

8. The clock repeater of claim 7, wherein said level detector means further comprises a first level detector means for detecting said high logical level and a second level detector means for detecting said low logical level of said clock signal.

9. The clock repeater of claim 8, wherein said first level detector means further comprising:

a low-threshold PMOS transistor and a high-threshold NMOS transistor for detecting said high logical level of said clock signal, wherein the gate of said low-threshold PMOS transistor and the gate of said high-threshold NMOS transistor being coupled together and to said clock signal, the drain of said low-threshold PMOS transistor being coupled to the drain of the high-threshold NMOS transistor, the source of said low-threshold PMOS being coupled to a supply voltage, and the source of said high-threshold NMOS transistor being coupled to an electrical ground; and

a first inverter having an input terminal coupled to the drain-drain junction of said low-threshold PMOS transistor and said high-threshold NMOS transistor to produce the said first signal, wherein the output terminal of said first inverter being the inverse of said first signal.

10. The regenerative clock repeater of claim 8, wherein said second level detector means further comprises:

a high-threshold PMOS transistor and a low-threshold NMOS transistor for detecting said low logical levels of said clock signal, wherein the gate of said high-threshold PMOS transistor and the gate of said low-threshold NMOS transistor being coupled together, the drain of said high-threshold PMOS transistor being coupled to the drain of the low-threshold NMOS transistor, the source of said high-threshold PMOS transistor being coupled to said supply voltage, and the source of said low-threshold NMOS transistor being coupled to said electrical ground; and

a second inverter having an input terminal coupled to the drain-drain junction of the high-threshold PMOS transistor and said low-threshold NMOS transistor to produce said second signal, wherein the output terminal which is the inverse of said second signal.

11. A synchronous semiconductor memory device, comprising:

a memory cell array including a plurality of memory cells arranged in rows and columns;

a data input/output terminal;

a control circuit controlling operations of said synchronous semiconductor memory device;

a sensing and writing circuit;

a row/column address decoder for selecting rows and columns of said memory cell array; and

a clock circuit for synchronizing said operations of said synchronous semiconductor memory device, wherein said clock circuit comprises a plurality

of regenerative clock circuits distributed along clock lines within said memory device, each of which further comprises:

(a) an edge detector means for sensing a rising edge and a falling edge of said clock signal and generating respective pull-up and pull-down control signals in response thereto;

(i) a level detector means for generating a first signal and a second signal by detecting a low logical level and a high logical level of said clock signal;

(ii) a first logic NOR gate adapted to receive an inverse of the first signal and an inverse of the second signal;

(iii) a second logic NOR gate adapted to receive the first signal and a second signal;

(iv) a set/reset latch coupled to an output of the first logic NOR gate at a set input terminal, and an output of the second logic NOR gate at the reset input terminal to produce a third signal;

(v) a first logic NAND gate adapted to receive the first signal, the inverse of the second signal to generate the pull-up control signal; and

(vi) a third logic NOR gate adapted to receive the inverse of the first signal, the second signal, and the third pulse signal to generate the pull-down control signal;

(b) an output driver means, connected to said edge detector means to receive said control signals therefrom, for recovering high and low logical levels of said clock signal;

(i) a pull-up PMOS transistor;

(ii) a NMOS pull-down transistor coupled to said pull-up PMOS transistor, wherein the gate of the said PMOS pull-up transistor being coupled to said pull-

up control signal, the drain of said pull-up PMOS transistor being coupled to the drain of the NMOS pull-down transistor and to said input clock signal, the source of the PMOS pull-up transistor being coupled to said voltage supply, a gate of the NMOS pull-down transistor being coupled to said pull-down control signal, and the source of said pull-down NMOS transistor coupled to said electrical ground.

12. The synchronous semiconductor memory device of claim 11, wherein said level detector means further comprises a first level detector means for detecting said high logical level and a second level detector means for detecting said low logical level of said clock signal.

13. The synchronous semiconductor memory device 12, wherein said first level detector means further comprising:

a low-threshold PMOS transistor and a high-threshold NMOS transistor for detecting said high logical level of said clock signal, wherein the gate of said low-threshold PMOS transistor and the gate of said high-threshold NMOS transistor being coupled together and to said clock signal, the drain of said low-threshold PMOS transistor being coupled to the drain of the high-threshold NMOS transistor, the source of said low-threshold PMOS being coupled to a supply voltage, and the source of said high-threshold NMOS transistor being coupled to an electrical ground; and

a first inverter having an input terminal coupled to the drain-drain junction of said low-threshold PMOS transistor and said high-threshold NMOS transistor

to produce the said first signal, wherein the output terminal of said first inverter being the inverse of said first signal.

14. The synchronous semiconductor memory device 7, wherein said second level detector means further comprises:

a high-threshold PMOS transistor and a low-threshold NMOS transistor for detecting said low logical levels of said clock signal, wherein the gate of said high-threshold PMOS transistor and the gate of said low-threshold NMOS transistor being coupled together, the drain of said high-threshold PMOS transistor being coupled to the drain of the low-threshold NMOS transistor, the source of said high-threshold PMOS transistor being coupled to said supply voltage, and the source of said low-threshold NMOS transistor being coupled to said electrical ground; and

a second inverter having an input terminal coupled to the drain-drain junction of the high-threshold PMOS transistor and said second low-threshold NMOS transistor to produce said second signal, wherein the output terminal which is the inverse of said second signal.

15. A method for regenerating a clock signal in a synchronous semiconductor memory, such method comprises the following steps:

detecting a rise edge from a low logical level and a fall edge from a high logical level of said clock signal;

generating a pull-up control signal in response to the detecting of the rise edge of the clock signal;

generating a pull-down control signal in response to the detecting of the fall edge of said clock signal;

recovering said high logical level using the pull-up control signal; and

recovering said low logical level using the pull-down control signal.

16. The method of claim 15 wherein the step of generating the pull-up control signal further comprises the steps of:

generating a first signal based on the high logical level;

generating a second signal based on the low logical level; and

generating a third signal using the first and the second signal and their complementary signals.